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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,748	02/10/2004	Klaus Goller	1890-0054	8728

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,748	GOLLER ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/17/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 12-20 are objected to because of the following informalities:

The claimed "a recess" in line 18 of claim 12, has an antecedent basis issue because there is already a recess claimed line 13 of claim 12. Is the limitation, "a recess," claimed in line 18 the same recess previously claimed, or is it a second recess? Claims 13-20 depend from claim 12 and thus contain the same error. The office will interpret the claimed recess in line 18 of claim 12 as a second recess.

The claimed "first dielectric layer" in line 15 of claim 12, lacks antecedent basis. Claims 13-20 depend from 12 and thus contain the same error. The office will interpret the claimed first dielectric layer as a dielectric layer beneath the second insulating layer.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12, 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 5,943,598) and Pasch et al. (US 6,239,491), in view of Jun et al. (US 6,064,119).

With respect to claim 12, Lin teaches (figs. 2a-2c):

An arrangement for contacting terminals of a substrate (10) comprising: a substrate surface, a first terminal (14b) having a first terminal surface, and a second terminal (14c) having a second terminal surface, the first terminal surface being located at a shorter distance from the substrate surface than the second terminal surface (Fig. 2a, col. 4, lns. 43-61), the arrangement comprising:

A first insulating layer (28) on the substrate surface, having an insulation-layer surface being located at a longer distance from the substrate surface than the second terminal surface, wherein a part of said first insulating layer is arranged between the first and the second terminal (Fig. 2a, col. 5, lns. 3-4).

a second insulating layer (38) arranged on the first insulting layer (28) (Fig. 2b, col. 5, lns. 49-55);

Wherein the first insulating layer (28) has a contact via (30d) which extends from the insulation-layer surface to the first terminal (14b) surface and is filled with a first conductive material (32d) (fig. 2b, col. 5, lns. 29-35); and

wherein the second insulating layer (38) has a recess (40c) penetrating the second insulating layer and extending to the first conductive material (32d) and into the first dielectric layer (34) (as best interpreted by the office) (fig. 2b, col. 5, lns. 56-62); and

being filled with a second conductive material (42) (fig. 2c, col. 6, lns. 6-14).

Furthermore it is inherent that the substrate, terminal, and insulation layers all have a surface.

Thus, Lin teaches the limitations set forth above in claim 12, but does not disclose:

wherein a recess extends to the second terminal surface through the first and second insulating layers, and is filled with a third conductive material.

However, Pasch teaches (fig. 3) a metal interconnection structure between insulating layers, wherein a recess (152 and 172) extends to the second terminal surface (132) through the first and second insulating layers (150 and 170), and is filled with a conductive material (col. 6, lns. 56-62; col. 8, lns. 55-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Lin to include a recess, filled with conductive material, extending to the second terminal surface through the first and second insulating layers, as taught by Pasch, for the disclosed intended purpose of forming vias with the same diameter through both insulating layers, thereby reducing the aspect ratio of the via, thereby reducing the number of steps required to manufacture the device, which improves efficiency and reduces cost of the process. Another advantage Pasch discloses is that a thinner photoresist mask can be used to form the recess, which in turn increases the resolution and accuracy of the pattern size and generally improve the masking process (col. 8, lns. 33-54).

Thus, Lin and Pasch are shown to teach all the limitations of the claim with the exception of disclosing:

that the second conductive material contacts the first conductive material on a top surface and on a portion of a side surface thereof.

However, Jun teaches a wiring structure in which a second conductive material (20) contacts a first conductive material (12) on a top surface and on a portion of a side surface thereof (fig. 2, col. 2, lns. 45-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Lin and Pasch to have the second conductive material contact the first conductive material on a top surface and on a portion of a side surface thereof, as taught by Jun, for the disclosed intended purpose of providing a wiring structure for a semiconductor device capable of minimizing the area of a conductive wire exposed through a misaligned contact hole, thereby maximizing the surface area of the first conductive material being exposed through the contact hole, thereby reducing a contact resistance and also obtaining a high reliability in semiconductor devices (col. 5, lns. 1-6).

With respect to claim 16, Pasch further teaches wherein at least one of the first conductive material, the second conductive material and the third conductive material comprises metal (column 7 lines 43-45).

With respect to claim 17, Pasch further teaches wherein the first conductive material is tungsten (column 7 lines 43-45).

With respect to claim 18, Pasch further teaches wherein at least one of the second conductive material and the third conductive material is copper (col. 8 lines 55-61).

With respect to claim 19, Pasch further teaches wherein the second conductive material (173) is conductively connected to first conductive material (154 and 134) and forms a first contact terminal, and wherein the third conductive material (172 and 152) is conductively connected to the second terminal (132) and forms a second contact terminal.

With respect to claim 20, Pasch further teaches wherein the first contact terminal (32' and 52') and second contact terminal (14 and 134 and 54') form a wiring plane (Fig. 2).

8. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin ('598), Pasch ('491) and Jun ('119) as applied to claim 12 above, and further in view of Cai et al. (6,830,966).

With respect to claim 13, Lin and Jun teach an arrangement for contacting terminals of a substrate as described in claim 12 above with the exception of explicitly disclosing:

The first terminal is one of a base terminal and a collector terminal, and the second terminal is an emitter terminal, arranged on a stack, of a bipolar transistor.

However, Cai teaches a device wherein the first terminal is one of a collector terminal (18), and the second terminal is an emitter terminal (26), arranged on a stack, of a bipolar transistor (column 5 lines 26-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the arrangement of contacting terminals of substrate as set

forth above to use the terminals for a bipolar transistor as taught by Cai because of the speed and precision of bipolar transistors.

With respect to claim 14, Cai teaches an arrangement of contacting terminals as set forth above in claim 12, wherein the first terminal is a drain terminal (18) and the second terminal is gate terminal (30) of a field-effect transistor (column 1 lines 8-10). It is well known in the art that an NMOS device is a field-effect transistor.

With respect to claim 15, Cai teaches an arrangement of contacting terminals as set forth above in claim 12, wherein the first terminal (18) is formed on the substrate (2) and is a collector terminal of a bipolar transistor (column 5 lines 26-28).

Response to Arguments

Applicant's arguments with respect to claims 12-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AK
4/28/06

ANH D. MAI
PRIMARY EXAMINER